THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 12

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ANTHONY M. BALISTRERI
and RICHARD SIMPSON

Appeal No. 97-0614
Application No. 08/212,465[1]

ON BRIEF

Before URYNOWICZ, THOMAS and FLEMING, Administrative Patent Judges.

URYNOWICZ, Administrative Patent Judge.

DECISION ON APPEAL

This appeal is from the final rejection of claims 1-12, all the claims pending in the application.

The invention pertains to a random access memory. Claim 9 is illustrative and reads as follows:

[1] Application for patent filed March 11, 1994. According to appellants, this application is a division of Application 07/676,624, filed March 28, 1991.

9. A random access memory comprising:

plural memory planes, each memory plane including:

N memory arrays;

N serial registers, each serial register coupled to a memory array;

N block write control circuits, each block write control circuit coupled to a memory array;

the random access memory further comprising:

a row address decoder, coupled to at least one of the memory arrays;

a column address decoder arranged for both block decoding and individual column decoding, the column address decoder being coupled to at least one of the memory arrays;

an address bus connecting with all of the memory arrays;

a data bus connecting with all of the memory arrays; and

the plural memory planes, the address bus, and the data bus are all fabricated on a single semiconductor substrate.

The reference relied upon by the examiner as evidence of obviousness is:

Pinkham et al. (Pinkham) 4,807,189 Feb. 21, 1989

The appealed claims stand rejected as under 35 U.S.C. § 102(b) as being anticipated by Pinkham.

The respective positions of the examiner and the appellants with regard to the propriety of these rejections are set forth in the final rejection (Paper No. 8), the examiner's answer (Paper No. 11) and the appellants' brief (Paper No. 10).

## Appellants' Invention

Appellants disclose a random access memory 100 having plural memory planes MP0-MP3. Each memory plane includes plural memory arrays MR00-MR03 having serial registers SR00-SR03, block write control circuits BWC00-BWC03 and row address decoder 153 coupled to the memory arrays. The random access memory further includes a column address decoder 58, an address bus 150, 155 and a data bus DQ0-DQ-15 coupled to the memory arrays. The memory planes, address bus and the data bus are all positioned on a single semiconductor substrate.

## The Prior Art

Pinkham discloses a random access memory having memory arrays 2. Serial registers 8, block write control circuit 24, 30,

row address decoder 18, and data and address buses D0-D7, A0-A8 are connected with the memory arrays.

The Rejection under 35 U.S.C. §102

Claims 1-12

Appellants have not specifically argued the patentability of any specific dependent claim, indicating how it defines appellants' invention over the prior art. Accordingly, appellant's claims stand or fall together. In re Nielson, 816 F.2d 1567, 2 USPQ2d 1525 (Fed. Cir. 1987).

After consideration of the positions and arguments presented by both the examiner and the appellants, we have concluded that the rejection should not be sustained.

There is but one issue in this case. The examiner contends that two or more memory arrays 2 of Pinkham may be considered as one memory plane[2]. Appellants argue that Pinkham does not disclose a plurality of memory planes with the planes all fabricated on a single semiconductor substrate.

[2] The designation “N” in “N memory arrays” which is in the claims is not defined in the claims. Accordingly, it is presumed that “N” may be 1.

The rejection must fail in that the examiner's assertion, that the reference has plural memory planes on a single semiconductor substrate because two or more memory arrays of Pinkham may be considered as one memory plane, is not accompanied by an explanation of why this is true. The examiner simply has provided no justification for his conclusion that two or more memory arrays of Pinkham may be considered as one memory plane, and thus, that the reference teaches plural memory planes fabricated on a single semiconductor substrate. It has not been established by any evidence what broadly constitutes a memory plane, nor has it been shown that two or more of Pinkham's memory arrays satisfy the definition of such a plane. Anticipation requires that all the elements of the claimed invention be described in a single reference. In re Spada, 911 F.2d 705, 708, 15 USPQ2d 1655, 1657 (Fed. Cir. 1990).

REVERSED

STANLEY M. URYNOWICZ, Jr. )
Administrative Patent Judge )
)
)
)

| | |
|---|---|
| | ) BOARD OF PATENT |
| JAMES D. THOMAS | ) APPEALS |
| Administrative Patent Judge | ) AND |
| | ) INTERFERENCES |
| | ) |
| | ) |
| | ) |
| MICHAEL R. FLEMING | ) |
| Administrative Patent Judge | ) |

SMU/gjh

Richard B. Havill
Texas Instruments Inc.
P.O. Box 655474, M/S 219
Dallas, TX 75265

***GJH***

Appeal No. 97-0614
Application No. 08/212,465

APJ URYNOWICZ

APJ THOMAS

APJ FLEMING

REVERSED

January 4, 2000